Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**LASER**

**ETCH**



**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .0025 x .0025”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .013” X .013” DATE: 12/15/22**

**MFG: SILICON SUPPLIES THICKNESS .007” P/N: 2SC3356**

**DG 10.1.2**

#### Rev B, 7/1